Wenhao Wang

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Education

Joint Institute of University of Michigan and Shanghai Jiao Tong University
Bachelor of Engineering in Electrical and Computer Engineering Sep. 2013 - Jul. 2017

School of Engineering and Applied Science of George Washington University
Master of Science in Electrical Engineering Sep. 2017 - Jun. 2019

College of Engineering of University of Illinois at Chicago
Research Assistant Aug. 2019 - Jul. 2020

College of Engineering of Northeastern University
Research Assistant Aug. 2020 - Dec. 2021

CISPA Helmholtz Center for Information Security
Ph.D. Student Apr. 2023 -

Research Experiences

Research on FPGA-based TRNG and delay line circuits design
Advisor: Professor Xiaolin Xu Sep. 2019 - Jun. 2020

Research on memory-based vulnerabilities
Advisor: Professor Xiaolin Xu Aug. 2020 till now

Research on microarchitectural vulnerabilities
Advisor: Professor Xiaolin Xu Aug. 2020 till now

Skills and Knowledge

- C / C++, Python, JAVA, Matlab, Verilog HDL
- Basic knowledge about Xilinx FPGA and related technologies, like hard-macros.
- Basic knowledge about network architecture (NDN, ICN, TCP/IP).
- Basic knowledge about microarchitectural vulnerabilities and memory-based vulnerabilities as well as corresponding attacks like CRAs, replay attack, prime & probe, etc.

Teaching Assistantship

ECE 465 Digital System Design (In UIC)
Advisor: Professor Xiaolin Xu 2020 Spring

Lab Section of ECE 225 Circuit Analysis (In UIC)
Advisor: Professor Jim Kosmach 2019 Fall

Publications & Awards

- Luo, Y. *, **Wang, W**. *, Best, S., Wang, Y. and Xu, X., 2020. A High-Performance and Secure TRNG Based on Chaotic Cellular Automata Topology. IEEE Transactions on Circuits and Systems I: Regular Papers, 67(12), pp.4970-4983. （* means equal contribution）
- Gong, Y., Zhan, Z., Li, Z., Niu, W., Ma, X., **Wang, W**., Ren, B., Ding, C., Lin, X., Xu, X. and Wang, Y., 2020, September. A privacy-preserving-oriented dnn pruning and mobile acceleration framework. In Proceedings of the 2020 on Great Lakes Symposium on VLSI (pp. 119-124).
- **W, Wang**., Luo, Y., and Xu, X., 2021, Constructive Use of Process Variations: Reconfigurable and High-Resolution Delay-Line. In Proceedings of 2021 on Design, Automation, and Test in Europe Conference (DATE 21).
- **W. Wang**, G. Hu, X. Xu and J. Zhang, "CRAlert: Hardware-Assisted Code Reuse Attack Detection," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 3, pp. 1607-1611, March 2022, doi: 10.1109/TCSII.2021.3118443.
- Shi, J., **Wang, W**., Luo, Y., and Xu, X., 2021, A Survey of Recent Attacks and Mitigation on FPGA Systems, In Proceedings of 2021 IEEE Computer Society Annual Symposium on VLSI (ISVLSI 21).
- Shi, J., Li, Z., Luo, Y., Sun, M., **Wang, W**., Lin, X., Xu, X., Chapter 5 of Book: Tehranipoor, M., 2021. Emerging Topics in Hardware Security. Springer Nature.
- **W, Wang** (Group leader)., Shi, J., Luo, Y., and Xu, X., Third place in the Embedded Security Challenges (ESC) of CSAW 21